Cleveland State University  
Department of Electrical Engineering and Computer Science  

EEC 580 Modern Digital Design  

**Catalog Data:**  
EEC 580 Modern Digital Design (4-0-4)  

*Prerequisite: Graduate standing*  
Coverage includes CPLD/FPGA devices, digital design methodology, VHDL hardware description language, VHDL description for combinational circuits, sequential circuits, FSM (finite state machine) and FSMD (finite state machine with datapath). No graduate credit for students who have completed EEC 487  

**Textbook:**  

**References:**  

**Course Coordinator:**  
Dr. Pong P. Chu,  
Associate Professor of Electrical Engineering and Computer Science.  

**Course Objectives:**  
To study the modern digital design methodology and usage of EDA tools and to use VHDL to describe and design combinational circuits, sequential circuits, FSM, and FSMD.  

**Expected Outcomes:**  
Upon completion, students should be able to  
- Understand the methodology and EDA tools used in modern digital system  
- Understand the synthesis flow  
- Design and synthesize combinational circuits using VHDL  
- Design and synthesize sequential circuits using VHDL  
- Design and synthesize FSM using VHDL  
- Design and synthesize FSMD using VHDL  

**Fulfillment of EE and CE Program Objectives and Outcomes**  

**Objectives:**  
(1) practice computer engineering  
(2) define and diagnose problems, and provide and implement computer engineering solutions in an industrial environment  

**Outcomes:**  
(a) an ability to apply knowledge of mathematics, science, and engineering to computer engineering  
(b) an ability to design and conduct computer engineering experiments, as well as to analyze and interpret data  
(c) an ability to design a system, component, or process to meet desired needs  
(k) an ability to use the techniques, skills, and modern engineering tools necessary for electrical engineering practice.  

**Prerequisites by Topic:**
• Boolean Algebra
• Basic logic gates and Karnaugh map
• MSI combinational components (adder, multiplexers, comparators etc.)
• MSI sequential components (registers, counters, etc.)
• Analysis and synthesis of FSM (finite state machine)

Course Outline:

Major Course Topics:
- Overview on modern digital design methodology (3)
- Overview on VHDL (3)
- VHDL object, data types and operators (3)
- Concurrent signal assignment for combinational circuit synthesis (6)
- Process statement for combinational circuit synthesis (4)
- VHDL for sequential logic synthesis (8)
- FSM (finite state machine) synthesis (4)
- FSMD (FSM with datapath) synthesis (2)
- Case study: UART (5)
- Case study: Ram based FIFO buffer (3)
- Test (3)

Total hours (44)

Major Lab Topics
- Introduction synthesis software (2)
- Combinational circuit (dual-priority encoder) (2)
- Arithmetic circuit (BCD addition circuit) (2)
- Sequential circuit (Programmable pulse generator) (2)
- FSM (2)
- UART (2)
- Project (4)

Total equivalent lecture hours (16)

Computer Usage: EDA software will be used in homework and lab experiment for VHDL entry, synthesis and simulation

Prepared by: Pong P. Chu Date: September, 2013