Cleveland State University  
Department of Electrical Engineering and Computer Science

EEC 487: Advanced Digital Systems

Catalog Data:  EEC 487 Advanced Digital Systems (3-0-3)  
Pre-requisite: EEC384  
Coverage includes CPLD/FPGA devices, digital design methodology, VHDL hardware description language, VHDL description for combinational circuits, sequential circuits, FSM (finite state machine) and FSMD (finite state machine with datapath).


Course Coordinator:  Dr. Pong P. Chu, Associate Professor of Electrical Engineering and Computer Science.

Course Objectives:  To study the modern digital design methodology and usage of EDA tools and to use VHDL to describe and design combinational circuits, sequential circuits, FSM, and FSMD.

Expected Outcomes:  Upon completion, students should be able to  
1. Understand the methodology and EDA tools used in modern digital system  
2. Understand the synthesis flow  
3. Design and synthesize combinational circuits using VHDL  
4. Design and synthesize sequential circuits using VHDL  
5. Design and synthesize FSM using VHDL  
6. Design and synthesize FSMD using VHDL

Fulfillment of EE and CE Program Objectives and Outcomes:  
Objectives:  (1) practice computer engineering  
(2) define and diagnose problems, and provide and implement computer engineering solutions in an industrial environment

Outcomes:  (a) an ability to apply knowledge of mathematics, science, and engineering to computer engineering  
(b) an ability to design and conduct computer engineering experiments, as well as to analyze and interpret data  
(c) an ability to design a system, component, or process to meet desired needs  
(k) an ability to use the techniques, skills, and modern engineering tools necessary for electrical engineering practice.

Contribution of Course to Meeting the Professional Component:  
Math & Basic Science: 0 credit;  
Engineering Topics: 4 credits;  
General Education: 0 credit

Prerequisites by Topic:  
Topics covered in EEC383 and EEC384
**Topics:**

**Major Course Topics**
- Overview on modern digital design methodology 3
- Overview on VHDL 3
- VHDL object, data types and operators 3
- Concurrent signal assignment for combinational circuit synthesis 6
- Process statement for combinational circuit synthesis 4
- VHDL for sequential logic synthesis 8
- FSM (finite state machine) synthesis 4
- FSMD (FSM with datapath) synthesis 2
- Test 2

**Total hours** 35

**Major Lab Topics**
- Introduction synthesis software 2
- Combinational circuit (dual-priority encoder) 2
- Arithmetic circuit (BCD addition circuit) 2
- Sequential circuit (Programmable pulse generator) 2
- FSM 2

**Total equivalent lecture hours** 10

**Computer Usage:** EDA software will be used in homework and lab experiment for VHDL entry, synthesis and simulation

**Laboratory Projects:** None

**Prepared by:** Pong P. Chu
**Date:** September, 2013